IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) An inspecting circuit of a semiconductor device comprising:

~~a plurality of input terminal which is inputted with signals from a plurality of~~ at least first and second signal lines ~~respectively~~; ~~and~~

at least first and second NANDs, each of the first and second NANDs having first and second input terminals; and

~~two~~ an output terminals ~~at which an~~ electrically connected to outputs of ~~inspection can be obtained~~ the first and second NANDs; [[,]]

wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND, and

wherein the second input terminals of the first and second NANDs are directly connected to first and second signal lines, respectively, and

wherein a determination whether the semiconductor device is normally operated or not is performed by ~~two signals~~ using at least a signal obtained at the ~~two~~ output terminals.

2. (Currently amended) The inspecting circuit of a semiconductor device according to claim 1, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

3. (Currently amended) The inspecting circuit of a semiconductor device according to claim 1, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

4. (Previously presented) The inspecting circuit of a semiconductor device according to claim 3, wherein an ExNOR is used for the comparator circuit.

5. (Currently amended) An inspecting circuit of a semiconductor device comprising;

~~a plurality of~~ at least first and second signal ~~output~~ lines;

~~a plurality of input terminals to which signals from a plurality of signal output lines are inputted; and~~

at least first and second NANDs, each of the first and second NANDs having first and second input terminals; and

an output terminal ~~at which an~~ electrically connected to outputs of ~~an inspection is obtained~~

the first and second NANDs,

wherein an output of the first NAND is electrically connected to the first input terminal of the second NAND, and

wherein the second input terminals of the first and second NANDs are directly connected to first and second signal lines, respectively, and

wherein a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained at the output terminal ~~by a signal inputted to the plurality of input terminals~~ and a reference pattern.

6. (Currently amended) The inspecting circuit of a semiconductor device according to claim 5, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

7. (Currently amended) The inspecting circuit of a semiconductor device according to claim 5, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically

connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

8. (Previously presented) The inspecting circuit of a semiconductor device according to claim 7, wherein an ExNOR is used for the comparator circuit.

9. (Currently amended) ~~An inspecting circuit of a~~ semiconductor device comprising:

a source driver which inputs a clock signal, a start pulse and a video signal and outputs a plurality of signals to a plurality of source signal lines in accordance with the clock signal, the start pulse and the video signal;

an inspecting circuit including a plurality of input terminals and an output terminal at which an output of an inspection is obtained,

~~to which~~ wherein the plurality of signals outputted to the plurality of source signals lines are inputted to the plurality of input terminals, ~~respectively; and~~

~~an output terminal at which an output of an inspection is obtained,~~

wherein a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained ~~by a signal inputted to the plurality of input terminals~~ at the output terminal and a reference pattern.

10. (Currently amended) The inspecting circuit of a semiconductor device according to claim 9, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

11. (Currently amended) The inspecting circuit of a semiconductor device according to claim 9, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

12. (Previously presented) The inspecting circuit of a semiconductor device according to claim 11, wherein an ExNOR is used for the comparator circuit.

13. (Currently amended) ~~An inspecting circuit of a~~ semiconductor device comprising:

a gate driver which inputs a clock signal and a start pulse and sequentially outputs a select pulse to a plurality of ~~source~~ gate signal lines in accordance with the clock signal and the start pulse;

an inspecting circuit including a plurality of latch circuits ~~sample~~ sampling a signal for

inspection in accordance with the select pulse ~~which is outputted sequentially to the plurality of gate lines; and,~~ a plurality of input terminals to which output signals from the plurality of latch circuits are inputted[[;]], and an output terminal at which an output of an inspection is obtained,

wherein a determination whether the semiconductor device is normally operated or not is performed by comparing an output pattern obtained at the output terminal ~~by a signal inputted to the plurality of input terminals~~ and a reference pattern.

14. (Currently amended) The inspecting circuit of a semiconductor device according to claim 13, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs; and

a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

15. (Currently amended) The inspecting circuit of a semiconductor device according to claim 13, the inspecting circuit further comprising:

a plurality of NANDs;

a plurality of NORs;

a plurality of inverters; and

a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal of a NOR of i-th line (i is an integer number of two or more) in the plurality of NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained; and

wherein an output terminal of the comparator circuit is electrically connected to an output

terminal at which an output of an inspection is obtained.

16. (Previously presented) The inspecting circuit of a semiconductor device according to claim 15, wherein an ExNOR is used for the comparator circuit.

17. (Currently amended) An inspecting circuit of a semiconductor device comprising:

a plurality of NANDs, a plurality of NORs, and a plurality of inverters,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to an output terminal at which a first output of an inspection is obtained; and

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to an output terminal at which a second output of an inspection is obtained.

18. (Currently amended) An inspecting circuit of a semiconductor device comprising:

a plurality of NANDs, a plurality of NORs, a plurality of inverters, and a comparator circuit,

wherein an output terminal of an NAND of i-th line (i is an integer number of two or more) in the plurality of NANDs is electrically connected to a first input terminal of a NAND of (i + 1)th line through one of the plurality of inverters;

wherein an output terminal a NOR of i-th line (i is an integer number of two or more) in the plurality or NORs is electrically connected to a first input terminal of a NOR of (i + 1)th line through another one of the plurality of inverters;

wherein the plurality of input terminals are electrically connected to second input terminals of the plurality of NANDs and second input terminals of the plurality of NORs respectively;

wherein an output terminal of a NAND of a final line in the plurality of NANDs is electrically connected to a first input terminal of the comparator circuit;

wherein an output terminal of a NOR of a final line in the plurality of NORs is electrically connected to a second input terminal of the comparator circuit; and

wherein an output terminal of the comparator circuit is electrically connected to an output terminal at which an output of an inspection is obtained.

19. (Previously presented) The inspecting circuit of a semiconductor device according to claim 18, wherein an ExNOR is used for the comparator circuit.

20. (Currently amended) An inspecting method of a semiconductor device comprising the steps of:

~~inputting signals outputted to all of a plurality of output signal lines to an inspecting circuit simultaneously;~~

simultaneously inputting a signal to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i-th NAND is inputted to a second input terminal of (i+1)th NAND;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.

21. (Currently amended) An inspecting method of a semiconductor device, comprising the steps of:

sampling signals for inspection sequentially in accordance with signals outputted sequentially from a plurality of output signal lines;

~~inputting all of the sampled signals for inspection to an inspecting circuit simultaneously;~~

simultaneously inputting each of the sampled signals to each first input terminal of n NANDs included in an inspecting circuit, wherein an output of i-th NAND is inputted to a second input terminal of (i+1)th NAND;

obtaining an output pattern from the inspecting circuit; and

determining an operation of the semiconductor device to be good or defective by comparing the output pattern and a reference pattern.